STATIC INDUCTION TRANSISTOR WITH DIELECTRIC CARRIER SEPARATION LAYER

FIELD OF THE INVENTION

[0001] The present invention relates to semiconductor devices and, in particular, to static induction transistor (SIT) designs that utilize a dielectric carrier separation layer to achieve a lower gate-to-source capacitance and also to prevent direct carrier injection from gate to source when the junction is forward biased. By placing a dielectric layer between the gate and the source, undesirable gate-to-source breakdown can be avoided at smaller gate-to-source separation.

BACKGROUND

[0002] As discussed in U.S. Pat. No. 4,326,209, issued on Apr. 20, 1982, to Nishizawa et al., a static induction transistor (SIT) is a field-effect semiconductor device that is capable of operation at relatively high frequency and power. A SIT is characterized by a short, high resistivity semiconductor channel region that may be controllably depleted of carriers. The current-voltage characteristics of a SIT are generally similar to those of a vacuum tube triode. Devices of this type are also described in U.S. Pat. No. 4,566,172, issued on Jan. 28, 1986, to Bencuya et al.

[0003] Referring to FIG. **1**, a SIT **100** generally utilizes vertical geometry with a source region **102** of a first conductivity type (n+ in FIG. **1**) and a drain region **104** of the first conductivity type (n+ in FIG. **1**) formed on opposite sides of a thin, high resistivity layer **106** of the first conductivity type (n in FIG. **1**). Gate regions **108** of a conductivity type (p+ in FIG. **1**) that is opposite the conductivity type of the source region **102** and the drain region **104** are positioned in the high resistivity layer **106** on opposite sides of the source region **102**. During operation, a reverse bias is applied between the gate regions **108** and the remainder of the high resistivity layer **106** causing a depletion region **110** to extend into the channel region that is formed below the source region **102** and between the gate regions **108**. As the magnitude of the reverse bias is varied, which in turn causes the extent of the depletion region **110** to vary, the electric field distribution and the resulting source-drain current will also vary. At large enough reverse bias on the gate, the adjacent depletion regions **100** merge, thus interrupting the source-to-drain current flow.

[0004] The most critical parameters in a SIT are the spacing between the gate regions **108** and the channel doping level N_D. Since most SITs are designed to be normally-on, the channel doping level N_D is chosen such that the depletion region **110** from the gate regions **108** does not merge and that there exists, as shown in FIG. **1**, a narrow, neutral channel opening **112** with zero gate bias. Typical gaps between the gate regions **108** are a few microns, with channel doping levels N_D in the 10^{15} cm^{-3} range. The FIG. **1** SIT structure **100** shows the gate regions **108** formed by p-n junctions, but the SIT operations can be generalized to include metal (Schottky) gates or MIS gates. Most SIT devices are fabricated on a silicon (Si) substrate, with gallium arsenide (GaAs) and silicon carbide (SiC) being the next material choices for higher speed operations.

[0005] As stated above, in normal mode, a SIT shows triode-like characteristics with high-linearity. A SIT also has a bipolar mode (BSIT). This occurs when the gate region is forward biased past the turn-on voltage of the gate-source junction. High current gains with large current densities are possible in the bipolar mode.

[0006] Despite their promise, however, the SIT and BSIT have not yet come into widespread use. This is because, in order to realize their full potential, SIT devices require non-standard processing that is unlikely to be found in standard foundry processes. The current foundry-centric model of production for integrated circuit devices has favored the adoption of power devices that can be fabricated utilizing more conventional processes, and which are thereby more easily monolithically integrable (e.g., LDMOS). Furthermore, conventional CMOS processes lack a good bipolar component. These CMOS processes additionally utilize thin oxides and, therefore, lack a transistor that can withstand a high off-state gate voltage.

[0007] Thus, there is a need in a CMOS process for a SIT device with higher gate voltage capability than can be provided by the thin gate oxides currently available. There is also a need for a bipolar-like device with good current gain, but without the extra cost imposed by utilizing a BiCMOS process. The SIT device needs to be fabricated utilizing unit steps used in standard processes to be compatible with the foundry-centric model. It also needs to be planar, since modern foundry processes have stringent planarity requirements.

SUMMARY

[0008] Embodiments of the present invention provide a static induction transistor comprising: a region of semiconductor material having a first conductivity type; at least two spaced-apart gate regions formed in the region of semiconductor material, the gate regions having a second conductivity type that is opposite the first conductivity type; at least one source region having the first conductivity type formed in the region of semiconductor material between the spaced-apart gate regions; a drain region having the first conductivity type formed in the region of semiconductor material and spaced-apart from the source region to define a channel region therebetween; and a dielectric carrier separation layer formed at the periphery of the gate regions.

[0009] The features and advantages of the various aspects of the subject matter disclosed herein will be more fully understood and appreciated upon consideration of the following detailed description and the accompanying drawings, which set for illustrative embodiments of the claimed subject matter.

BRIEF DESCRIPTION OF THE DRAWING

[0010] FIG. **1** is a cross section drawing illustrating a conventional planar static induction transistor (SIT).

[0011] FIG. **2** is a cross section drawing illustrating an embodiment of an N-type static induction transistor (NSIT) in a conventional CMOS process.

[0012] FIG. **3** is a graph showing the output I_D-V_D characteristics of the FIG. **2** NSIT, as measured on an experimental device in CMOS implementation.

[0013] FIG. **4** is a graph showing the output I_D-V_D characteristics of the FIG. **2** NSIT in bipolar-mode operation, as measured on an experimental device in CMOS implementation.

[0014] FIG. **5** is a cross section drawing illustrating an alternate embodiment of an NSIT.